Notice of Allowability	Application No.	Applicant(s)	
	09/661,919	UCHINO, TAKU	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *19 October 2005*.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☒ The drawings filed on *12 September 2000* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

DETAILED ACTION

1. Claims 1-18 are currently pending in this application and have been presented for examination based on applicant's amendment filed 19 October 2004. Claims 1-18 have now been allowed over the prior art of record.

Response to Arguments

2. Applicant's arguments filed 19 October 2004 have been fully considered and found to be persuasive.

Regarding applicant's response to 112(1) rejection: The examiner withdraws the 101 rejection in view of applicant's amendment to the claims and arguments filed 19 October 2004.

Regarding applicant's response to 102(b) rejection: The examiner withdraws the 102(b) rejection in view of applicant's amendment to the claims and arguments filed 19 October 2004.

Allowable Subject Matter

3. Claims 1-18 have been allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

Applicants are disclosing a method and computer code for estimation power consumption and noise levels of an integrated circuit using occurrence probabilities. This has been disclosed in the prior art of record.

While these features are individually disclosed in the prior art, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ***ipsissimis verbis*** *test, i.e., identity of terminology is not required.* ***In re Bond****, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."*

In particular, the prior art of record does not disclose the specific sequence of steps relating to calculating a first, second, and n-th set of signal elementary waveforms and occurrence probabilities and subsequently estimating power consumption and noise levels based on n sets of output signal elementary waveforms and occurrence probabilities, in the context of the claims.

The closest prior art uncovered during examination is:

U.S. Patent 5,847,966 issued to Uchino et al: teaches estimating IC power consumption and noise level and calculating first, second, and n^{th} stage output waveform and occurrence probabilities.

U.S. Patent 5,557,531 issued to Rostoker et al: teaches IC power estimation using probabilities.

Specifically, while the prior art of record discloses various techniques for estimation of IC power consumption and noise level in integrated circuits using probabilities, it does not explicitly disclose the specific sequence of steps, relating to calculating a first set of signal elementary waveforms and occurrence probabilities at the

first stage primary terminals, calculating a second set of signal elementary waveforms and occurrence probabilities at the second stage primary terminals (and first set), calculating an n-th set (natural number) elementary waveforms and occurrence probabilities at the n-th stage of logic gates (n-1th set elementary waveforms), and subsequently estimating power consumption and noise levels based on the at least n sets of output signal elementary waveforms and occurrence probabilities, as now recited in independent claims 1, 7, and 13. (See: Fig. 5) This feature renders the claimed invention non-obvious over the prior art of record. Claims 2-6, 8-12, and 14-18 are deemed allowable as being dependent from independent claims 1, 7, and 13 respectively.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the

examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

Fred Ferris. Patent Examiner
Simulation and Emulation, Art Unit 2128
U.S. Patent and Trademark Office
Randolph Building, Room 5D19
401 Dulany Street
Alexandria, VA 22313
Phone: (571-272-3778)
Fred.Ferris@uspto.gov
February 16, 2005